What is claimed:

1. A method of making a semiconductor device having aluminum alloy lines over aluminum alloy plugs without forming plug recesses comprising:

forming a first metal layer on a substrate;

forming a dielectric layer over the first metal layer;

defining a via in the dielectric layer of sufficient depth to expose the first metal layer;

forming an aluminum alloy plug in the via;

forming a second metal layer over the aluminum alloy plug;

etching the second metal layer with a first etch chemistry;

changing to a second etch chemistry, wherein the etch rates of the second metal layer and the exposed dielectric layer, as provided by the second etch chemistry are approximately equal; and

over etching the second metal layer using the second etch chemistry.

2. The method as recited in claim 1 wherein over etching the second metal layer comprises etching a portion of the aluminum plug, not covered by the second metal layer, substantially flush with the surrounding dielectric.

3. The method as recited in claim 1 wherein the first etch chemistry comprises a chlorine-based chemistry and the second etch chemistry comprises a fluorine-based chemistry.

4. The method as recited in claim 1 wherein the first etch chemistry is selected from the group of HCl, Cl_2 and BCl_3 and the second etch chemistry is selected from the group of SF_6, CF_4, CHF_3, and C_2F_6.

5. The method as recited in claim 1 wherein the second etch chemistry has a selectivity ratio of 1:1 for the aluminum alloy and the dielectric.

6. The method of claim 1 wherein the first etch chemistry comprises a chemistry selected from the group of HCl, Cl_2 and BCl_3 combined with at least one gas from the group of N_2, Ar and CHF_3.

7. A method of making a semiconductor device having aluminum alloy lines over aluminum alloy plugs without forming plug recesses comprising:

forming a first metal layer on a substrate;

forming a dielectric layer over the first metal layer;

defining a via in the dielectric layer of sufficient depth to expose the first metal layer;

depositing a barrier layer substantially conforming to the via;

forming an aluminum alloy plug in the via and;

forming a second metal layer over the aluminum alloy plug;

etching the second metal layer with a first etch chemistry;

changing to a second etch chemistry, wherein the etch rates of the second metal layer, the exposed dielectric layer, and the barrier layer, as provided by the second etch chemistry are approximately equal; and

over etching the second metal layer using the second etch chemistry.

8. The method as recited in claim 1 wherein over etching the second metal layer comprises etching portions of the aluminum plug and barrier layer, not covered by the second metal layer, substantially flush with the surrounding dielectric.

9. The method as recited in claim 7 wherein the second etch chemistry has a selectivity ratio of 1:1:1 for the aluminum alloy, barrier metal, and the dielectric.

10. The method as recited in claim 7 wherein the first metal layer and the second metal layer comprise aluminum alloys electrically coupled with the barrier layer.

11. The method of claim 7 wherein the first etch chemistry comprises a chemistry selected from the group of HCl, Cl_2 and BCl_3.

12. The method of claim 7 wherein the first etch chemistry comprises a chemistry selected from the group of HCl, Cl_2 and BCl_3 combined with at least one gas from the group of N_2, Ar and CHF_3

13. The method of claim 7 wherein the barrier layer is comprised of a metal selected from the group of titanium, tantalum, tungsten, and molybdenum.

14. A method of making a semiconductor device having aluminum alloy lines over aluminum alloy plugs without forming plug recesses comprising:

forming a first metal layer;

forming a dielectric layer over the first metal layer;

defining a via in the dielectric layer of sufficient depth to expose the first metal layer;

forming an aluminum alloy plug in the via;

forming a second metal layer;

etching the second metal layer with a first etch chemistry selected from the group of HCl, Cl_2 and BCl_3;

changing the etch chemistry to a second etch chemistry by selecting the etch chemistry from the group of SF_6 and CF_4, CHF_3, C_2F_6, wherein the etch rates of the second metal layer and the exposed dielectric layer, as provided by the second etch chemistry are approximately equal; and

over-etching the second metal layer with the second etch chemistry such that a portion of the aluminum plug not covered by the second metal layer is etched substantially flush with the surrounding dielectric.

15. A method of etching a semiconductor device having aluminum alloy lines over aluminum alloy plugs surrounded by a dielectric layer and electrically coupled to a lower level metal layer, comprising:

placing one or more wafers inside a plasma etch reactor chamber;

reducing the chamber pressure until vacuum is achieved;

performing a bulk etch of the aluminum alloy lines and aluminum alloy plugs;

performing an endpoint etch of the aluminum alloy lines and aluminum;

performing a residue etch of the aluminum alloy lines and aluminum plugs;

performing an over-etch of the aluminum alloy lines and aluminum alloy plugs wherein the etch rates of the aluminum alloy lines and the dielectric layer, as provided by the over etch are approximately equal; and

breaking vacuum so that wafers can be removed from the plasma etch reactor chamber.

16. The method as recited in claim 15 wherein the aluminum alloy plugs are surrounded by a barrier layer.

17. The method as recited in claim 16 wherein performing an over-etch of the aluminum alloy lines and aluminum alloy plugs comprises etching portions of the aluminum alloy plugs and the barrier layer, not covered by the aluminum alloy lines, substantially flush with the surrounding dielectric layer.

18. The method as recited in claim 16 wherein the barrier layer is comprised of a metal selected from the group of titanium, tantalum, tungsten, and molybdenum.

19. A method of etching a semiconductor device having aluminum alloy lines over aluminum alloy plugs surrounded by a dielectric layer and a barrier layer and electrically coupled to a lower level metal layer, comprising:

placing one or more wafers inside a plasma etch reactor chamber;

reducing the chamber pressure until vacuum is achieved;

performing a bulk etch of the aluminum alloy lines and aluminum alloy plugs;

performing an endpoint etch of the aluminum alloy lines and aluminum;

performing a residue etch of the aluminum alloy lines and aluminum plugs;

performing an over etch of the aluminum alloy lines and aluminum alloy plugs wherein the etch rates of the aluminum alloy lines, the dielectric layer and the barrier layer, as provided by the over etch are approximately equal; and

breaking vacuum so that wafers can be removed from the plasma etch reactor chamber.

20. The method as recited in claim 19 wherein the barrier layer is comprised of a metal selected from the group of titanium, tantalum, tungsten, and molybdenum.

21. The method as recited in claim 15 wherein performing the bulk etch of the aluminum alloy lines includes:

- introducing BCl_3 and Cl_2 at a flow rate of about 30 to 40 sccm for each species and maintaining chamber pressure to a range of about 9 to 12 mT for about 30 seconds; and
- etching the aluminum alloy lines for about 20 to 28 seconds at an RF-Top Power between 300 and 415 watts and an RF-Bottom Power between 85 to 115 watts;

wherein the performing the endpoint etch includes:

- etching for about 42 to 58 seconds at an RF Top Power between 300 and 415 watts and an RF Bottom Power between 190 to 260 watts until a trigger value of indicating AlCu clearing is reached;

wherein the performing the residue etch includes:

- changing the BCl_3 and Cl_2 flow rates to a range 43 to 58 sccm and to a range of 25 to 35 sccm, respectively and etching for about 3 to 7 seconds; and

wherein performing the over etch includes:

- introducing SF_6 at a flow rate of 17 to 23 sccm and etching for about 43 to 58 seconds.

22. The method as recited in claim 19 wherein performing the bulk etch of the aluminum alloy lines includes:

- introducing BCl_3 and Cl_2 at a flow rate of about 30 to 40 sccm for each species and maintaining chamber pressure to a range of about 9 to 12 mT for about 30 seconds; and
- performing a TiN and AlCu bulk etch for about 20 to 28 seconds at an RF-Top Power between 300 and 415 watts and an RF-Bottom Power between 85 to 115 watts;

wherein the performing the endpoint etch includes:

- performing an AlCu endpoint etch for about 42 to 58 seconds at an RF Top Power between 300 and 415 watts and an RF Bottom Power between 190 to 260 watts until a trigger value of indicating AlCu clearing is reached;

wherein the performing the residue etch includes:

- changing the BCl_3 and Cl_2 flow rates to a range 43 to 58 sccm and to a range of 25 to 35 sccm, respectively and performing a copper residue etch for about 3 to 7 seconds; and

wherein performing the over-etch includes:

introducing SF_6 at a flow rate of 17 to 23 sccm and performing a Ti+ 1:1:1 over etch for about 43 to 58 seconds.

23. A method of etching a semiconductor device after the formation of aluminum alloy lines over aluminum alloy plugs coupled to a lower level metal layer without forming plug recesses comprising:

placing one or more wafers inside a plasma etch reactor chamber;

reducing the chamber pressure until vacuum is achieved;

introducing BCl_3 and Cl_2 at a flow rate of about 30 to 40 sccm for each species and maintaining chamber pressure to a range about 9 to 12 mT for about 30 seconds;

performing a TiN and AlCu bulk etch for about 20 to 28 seconds at an RF-Top Power between 300 and 415 watts and an RF-Bottom Power between 85 to 115 watts;

performing an AlCu endpoint etch for about 42 to 58 seconds at an RF Top Power between 300 and 415 watts and an RF Bottom Power between 190 to 260 watts until a trigger value of indicating AlCu clearing is reached;

changing the BCl_3 and Cl_2 flow rates to a range 43 to 58 sccm and to a range of 25 to 35 sccm, respectively and performing a copper residue etch for about 3 to 7 seconds;

introducing SF_6 at a flow rate of 17 to 23 sccm and performing a Ti+ 1:1:1 over-etch for about 43 to 58 seconds; and

shutting off the flow of etchant gases and allowing chamber to pump down to vacuum; and

breaking vacuum so that wafers can be removed from the plasma etch reactor chamber.

24. A semiconductor device manufactured according the method of claim 1

25. A semiconductor device manufactured according to the method of claim 7.

26. A semiconductor device manufactured according the method of claim 14

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